

Application Serial No. 10/604,176

**REMARKS**

Claims 1-19 are pending in the present application. Claims 3 and 9 have been amended.

Applicant respectfully requests reconsideration of the application in view of the foregoing amendments and remarks appearing below.

**Rejection Under 35 U.S.C. § 112, Second Paragraph**

Claims 3 and 9 have been rejected under 35 U.S.C. § 112, second paragraph, based on insufficient antecedent basis for the phrase "said voltage potential" in these claims. Claims 3 and 9 have been amended to address this issue, and so withdrawal of this rejection is respectfully requested.

**Objection**

For reasons not specifically identified (no statute, rule or regulation has been cited), claims 7, 9, 12 and 17 have been objected to based on use of the term "active clamp network." Applicant believes the term "active clamp network" is used in the above-identified application, including claims 7, 9, 12 and 17, in accordance with its ordinary meaning in the technical field in which the claimed invention resides, as discussed more below. But assuming, *arguendo*, this is not the case, Applicant has clearly defined the meaning of "active clamp network" in the above-identified application. See, e.g., paragraphs 37, 38, 40 and FIGS. 3 and 4. Nor is there a suggestion to the contrary in the Office Action. The Office Action only identifies the conditions under which Applicant may act as his or her own lexicographer, it does not indicate that the written description fails adequately describe the meaning of "active clamp network."

"Active clamp network" has a specific meaning in the technical context of the claimed invention that differs from the meaning quoted in the Office Action from the Authoritative Dictionary of IEEE Standard Terms, 7<sup>th</sup> Ed., 2000. An active clamp network turns on beyond the normal power supply range of operation at the edges of the VSS and VDD power supply. Active clamp networks are typically a zero threshold device which is initiated at the extremities of the power supply voltages. Examples of use of "active clamp network" in accordance with this meaning

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includes U.S. Patent No. 6,075,399 and U.S. Patent No. 6,229,372. The opportunity to act as one's own lexicographer does not apply to the U.S. Patent and Trademark Office. As such, it is inappropriate to redefine "active clamp network" as "a circuit that adds a fixed bias to a wave at each occurrence of some predetermined feature of the wave so that the voltage or current of the features is held at, or 'clamped' to some specified level." Instead, the "active clamp network" of the present invention is an always-active network which de-couples the power supply rails of the sea of gates (e.g., P-channel MOSFET to VDD and N-channel MOSFET to VSS) from its power supplies.

Applicant has used "active clamp network" in a manner that is conventional in the technical field of the claimed invention. Moreover, Applicant has described the "active clamp network" in a way that is sufficient to permit Applicant to act as his own lexicographer relative to this term (although Applicant believes this is not the case here). For these reasons, the objection to claims 7, 9, 12 and 17 is respectfully traversed, and favorable reconsideration is requested.

#### Rejection Under 35 U.S.C. § 103

Claims 1-19 have been rejected under 35 U.S.C. § 103(a) in view of various combinations of references. Before discussing the various rejections in detail, a few preliminary comments are needed. As a general matter, the various references applied in the rejections are drawn from such different technical fields that combining them in the manner suggested in the Office Action will create inoperative structures. Further, some of the references are drawn from technology fields that are irrelevant to the claimed invention. The various rejections have been assembled in an effort to try and develop a *prima facie* showing of obviousness. Unfortunately, as discussed below, because of the large disparity in the fields of invention of the references applied in the rejections, and because several of these references are not even relevant to the field of technology of the claimed invention, no *prima facie* showing of obviousness has been made.

Claim 1 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Li et al. (USP 6,624,660) in view of Lin et al. (USP 6,473,282) and Miyamoto (USP 4,905,199). Li et al.

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teaches a mixed voltage floating well output driver. All mixed voltage interface driver networks are inherently latchup immune in a CMOS output driver. As such, as a starting point, the Li et al. reference is not believed to be relevant to the field of technology at issue in claim 1. The portion of the Li et al. reference cited in the Office Action, i.e., col. 6, lines 36-67, is silent regarding use of latchup control isolation network, contrary to the assertion in the Office Action. This is not surprising given the inherent latchup immunity of the Li et al. invention. Nor do Li et al. disclose an active clamp network in the manner described by Applicant. As discussed above, a switching off network is not an active clamp network in the sense used by Applicant.

Lin et al. is directed to a system for sequencing a dual power supply environment between two common power supplies, i.e., VDD rails, to prevent latchup. Without considering whether or not Lin et al. teach the "sea of gates" connections recited in claim 1, it is inappropriate to combine the mixed voltage interface output driver of Li et al. with a "sea of gates." The "sea of gates" is not a mixed voltage interface output driver design environment. As such, no motivation or suggestion exists to combine Li et al. and Lin et al. to provide the invention of claim 1. One skilled in the art, therefore, would not make this combination.

Miyamoto is directed to a circuit for sequencing a back bias network and the substrate. The back bias network of Miyamoto is the cause of the latchup concern and is not equivalent to the sea of gates environment recited in claim 1. As such, one skilled in the art would not be motivated to combine the Miyamoto reference with the Li et al. and Lin et al. references so as to achieve the invention of claim 1. Indeed, just the opposite is true. A DRAM and the back-bias generator of Miyamoto cannot be extrapolated to the sea of gates environment defined in claim 1.

Considered together, the Li et al., Lin et al. and Miyamoto references are not properly combinable as they are directed to very different inventions, both as compared to claim 1 and as between the inventions disclosed in these patents. As a result, nothing in the working knowledge of one skilled in the art nor within the four corners of these patents suggests combining the teachings thereof in a way that anticipates the invention of claim 1. For this reason, Applicant requests favorable reconsideration of this claim.

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Claims 7 and 12 have also been rejected in view of the Li et al./Lin et al./Miyamoto combination and further in view of Blossfield (USP 5,530,394). Blossfield does not remedy the deficiencies of the Li et al./Lin et al./Miyamoto combination discussed above. Blossfield does not separate the circuitry from the power supply rails VDD and VSS and hence is not applicable to the concept of latchup in the context of the present invention. Indeed, latchup can still occur with the Blossfield invention because the sub-circuits are not electrically isolated from the VDD and VSS power supply rails. Latchup occurs through the parasitic nodes electrically connected to the power supply and has nothing to do with the internal nodes. As discussed above relative to the objection to claims 7, 9, 12 and 17, an active clamp network is not a switching off circuit. Blossfield was applied for its teaching of a switching off circuit. In summary, Blossfield does not address the latchup from power supply overshoot, does not decouple the sea of gates circuits, and does not teach or suggest an active clamp network. For these reasons, and for the reasons discussed above relative to claim 1, claims 7 and 12 are believed to be patentable over the Li et al./Lin et al./Miyamoto/Blossfield combination, and so favorable reconsideration is requested.

Concerning the rejection of claims 3, 9, 14 and 17, as noted above, Li et al. does not disclose a latchup control isolation network. The mixed voltage output driver circuit of Li et al. does not "isolate said sea of gates from said power rail in response to latchup events on said substrate," as recited in claim 1, as no sea of gates is believed to exist and latchup is not a concern of the invention. For these reasons, claims 3, 9, 14 and 17 are believed to be patentable, and favorable reconsideration of the rejection is requested.

As to the rejection of claims 4, 10, 15 and 18, claims 4, 10 and 18 do not recite VDD+VBE. As to claim 15, this claim depends on claim 12, which is patent for the reasons discussed above. For these reasons, Applicant respectfully traverses the rejection of claims 4, 10, 15 and 18 and requests favorable reconsideration.

Regarding claims 2, 5, 6, 8, 11, 13, 16 and 19, these claims are patentable at least because they depend on independent claims that are patentable for the reasons discussed above. Accordingly, Applicant requests favorable reconsideration of these claims.

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**CONCLUSION**

In view of the foregoing, Applicant submits that claims 1-19, as currently presented, are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,  
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